A comparative analysis of the location behaviour of the US and European semiconductor manufacturers

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Abstract

Our paper analyses micro-level data from the US and European semiconductor manufacturers. In particular, we will focus on the plants undertaking the wafer manufacturing processes. We integrate a range of production technological indices with spatial data and regional economic variables in order to understand the issues determining the location behavior of the industry. Our results indicate that the locational behaviors of the US and European wafer plants do not correspond to an orthodox product-life-cycle model.

1. Introduction

Much of the current literature on hi-tech developments within the electronics industry tends to focus on the spatial and organisational arrangements evident in innovative clusters such as Silicon Valley. There are, however, many very different forms of spatial organisation which engender innovations within the semiconductor industry, and these variations depend on the particular sub-sector of the semiconductor industry. In this paper we discuss the case of US and European semiconductor producers. The paper will analyse data from over 100 semiconductor plants operated by over 50 firms located within the US and Europe. In particular, we will focus on the firms undertaking the wafer manufacturing processes. As we will see in this paper, in order to discuss the geographical behaviour of many parts of the semiconductor industry, it is necessary to consider not only organizational issues, but also the different sub-sectors within the industry. From these perspectives, many of the generalizations made about the semiconductor industry based on observations of Silicon Valley are seen to be rather inappropriate.

This paper is organized as follows. In section 2 we review the types of arguments frequently associated with discussions about the spatial organization of the semiconductor industry and spatial patterns of innovation. In section 3, we describe the three different components of the semiconductor industry. As we will see, many of the issues raised in section 2 really only relate to one sub-sector of the electronics industry, and the two other parts of the industry have been almost entirely ignored in the literature. In section 4 we discuss our detailed indices of product innovations within the

wafer-processing sub-sector of the industry, and we estimate relationships between geographical, firm and technological variables within a product-cycle framework. We find very little support for a product-cycle type model. In order to account for these findings, in section 5 we explore the organizational issues governing the spatial patterns of product innovations within the semiconductor industry.

2. Geography and the semiconductor industry

Over the last decade there has been a significant growth in interest in the geographical behaviour of firms in the electronics and semiconductor industry (Oakey and Cooper 1989; Saxenian 1994; Almeida and Kogut 1997; Kittiprapas and McCann 1999). There are a variety of interrelated reasons for this recent research interest, which can broadly be grouped into three themes. The first theme is a general renewal of academic interest in geography and industrial location issues per se. This has been encouraged in part by the continuing process of economic integration in many parts of the world, such as the EU and NAFTA, as well as by the writings of certain influential commentators (Porter 1990; Krugman 1991). The second theme is a growth in interest in the particular characteristics of the electronics and semiconductor industry itself. The reason for this is partly that electronics, and in particular the semiconductor part of the electronics industry, is generally regarded as an industry which is both highly successful, and also at the forefront of human technological development (Piore and Sabel 1984; Best 1990). At the same time, innovations in this industry are often embodied into the production technology of other industries, thereby having induced productivity effects. Therefore, it is implicitly assumed that observation of the behaviour of the electronics and semiconductor sector may also provide clues as to the future trajectory of other industrial sectors in general. A third reason for the growth in interest in the electronics and semiconductor industry has been the apparent tendency of this industry to cluster in particular locations such as Silicon Valley (Scott 1988, 1991: Saxenian.1994; Angel 1991). The result of this behaviour is that certain areas appear to exhibit high growth performance in this sector, while other areas have been unable to develop any equivalent industry base (***The Economist*** 1997). This has lead to concern among public policy planners in various countries and regions (Castells and Hall 1994) to understand the economic-environmental conditions under which such industrial clusters are fostered, in the hope of replicating these conditions elsewhere.

In order to generate such an array of new product developments, these combined features are assumed to imply that the semiconductor industry will also tend to be at the forefront of organizational developments (Eisenhardt and Schoonhaven 1990) and

production process innovations (McCann and Fingleton 1996). Therefore, observation of the current organizational behaviour of the semiconductor industry may point towards the future behaviour of industry in general, as other industrial sectors attempt to imitate the successful organization and production innovations exhibited by this sector. Indeed, much of the current thinking about the optimal relationship between industry organization and geography has been developed on the basis of observations of the large numbers of small and medium sized semiconductor firms in locations such as Silicon Valley (Saxenian 1994; Scott 1988, 1991; Larsen and Rogers 1984). In many circles (Keeble and Wilkinson 1998) it has now become almost a matter of faith that many small and medium sized firms clustered at the same location will guarantee the maximum levels of product innovation (Aydalot and Keeble 1988; Saxenian 1994). The logic behind this argument is that such small firms are assumed to find it not only relatively easy to share information and to benefit from local information spillovers, but also to reconfigure their organizational and input-output linkages appropriately as new product developments occur. Empirical support for these arguments, which appears to confirm the local presence of industry-specific informal information spillovers, comes primarily from patent citation counts (Jaffe et al. 1993; Almeida and Kogut 1997). Meanwhile, these observations of the high growth performance of small firm clusters such as Silicon Valley (Saxenian 1994), Cambridge UK (Castells and Hall 1994) and Ile de France (Scott 1988) are contrasted with the relatively weaker growth performance of the large-firm parts of the electronics industry (Saxenian 1994). Explanations for the apparent difference in the growth performance of the small and large firm sectors, are based on the assumptions that the organizational rigidity and well-defined boundaries of large hierarchical firms, limit the ability of large firms to respond appropriately to the rapid market changes of these new industries (Saxenian 1994). Small firm clusters are therefore perceived to represent the future optimal spatial and organizational arrangements in industries with very short product life cycles (Piore and Sabel 1984; Porter 1990; Saxenian 1994).

Such arguments, however, are based on very strong assumptions about the relationship between information generation, information exchanges and geographical scales. Following Marshall (1920) and Vernon (1960), the clustering argument is based on the assumption that information spillovers are generated and realised specifically at the geographical scale of the local urban area. Urban clustering is therefore advantageous for industries which exhibit very short product life-cycles (Vernon 1966, 1979). Yet, recent research within the electronics and semiconductor industry (Suarez-Villa and Rama 1996; Suarez-Villa and Karlsson 1996; Wever and Stam 1988)

suggests that agglomeration linkages, and the formal outcomes of any informal information spillovers (Audretsch and Feldman 1996; Suarez-Villa and Walrod 1997; Arita and McCann 2000) extend over much larger spatial scales than that of the individual urban metropolitan area. In the case of multi-plant multinational firms (Cantwell and Iammarino 2000), any such agglomeration effects may even operate over spatial scales larger than individual countries. These empirical observations therefore cast doubt on the assumed importance of specifically local inter-firm information spillovers as a source of competitive advantage (Porter 1990, 1998) within the electronics industry, and point rather more to the role of labour market hysteresis as a possible rationale for industrial clustering (Angel 1991; Arita and McCann 2000). More importantly, however, these observations also cast doubt on the whole hypothesis that small firm clusters represent something of an ideal spatial and organizational arrangement ensuring the maximization of innovation, either for the semiconductor industry or any other innovative industry facing short product life-cycles.

Part of the problem here is that so much of the literature which purports to show a high correlation between spatial industrial clustering, small and medium sized firms and short product life-cycles, has tended to focus on the spatial and organizational issues of only one particular part of the global electronics and semiconductor industry. The electronics industry as a whole is comprised of many sub-sectors ranging from the semiconductor industry to the consumer electronics sectors, and the semiconductor industry itself is comprised of three quite distinct sub-sectors, defined in terms of the nature of the activities and the transactions they undertake. Observations of Silicon Valley and the 'Cambridge Phenomenon' (Castells and Hall 1994) are actually primarily observations of groups of small firms whose activities correspond solely to only one of the three sub-sectors within the semiconductor industry, namely the Design sector. Yet, there are also many large vertically-integrated firms in this same sub-sector of the industry which are almost entirely ignored by the literature. Similarly, the other two parts of the semiconductor industry, the Wafer Process and the Wafer Manufacturing sectors, are characterized almost entirely by vertically-integrated wafer manufacturing and assembly firms. The spatial and organizational arrangements of the vertically-integrated parts of the semiconductor are completely different to the small semiconductor firms (Arita and McCann 2002a,b). The relationships between geography and technology within the semiconductor must therefore be considered individually for each of the three sub-sectors of the industry. Only in this way can we assess whether or not the types of spatial and organizational arrangements of Silicon Valley are more generally applicable to the parts of the industry.

Firm location behaviour within the semiconductor industry is often the result of different, and sometimes conflicting objectives. Rarely is the geographical result in reality a Silicon Valley-style spatial clustering of highly innovative small firms generating very short product life-cycle outputs. This is partly why such high-technology clusters are of interest, but also it is why generalizations based on such observations should be avoided. In order to appreciate these points we must first discuss the nature and organization of the semiconductor industry itself.

3.The Organization of the Semiconductor Industry

In order to understand the organization of the semiconductor industry it is first necessary to understand the different activities which take place within the industry (Nishimura 1995, 1999; EIAJ 1994). As we see in Fig.1, the different activities in the semiconductor industry can be compared more or less directly with the different activities which take place in the book publishing industry.

The first stage of the production process is the silicon chip design stage, in which the functional logic of the chip, and three-dimensional circuit layout of transistors and capacitors within the silicon wafer is determined. This activity is carried out primarily using computer aided design (CAD) systems. This stage of the process can be compared with the planning, editing and layout stages of the book publishing process. The result of this stage is the production of masks, which are the three-dimensional templates of the chip. These Integrated Circuit (IC) design activities are undertaken both by the large number of small specialized IC design firms, and also by large vertically-integrated semiconductor producing firms. The activities are provided for by specialist CAD vendor firms which provide customized design software for the designers. At the same time, there has also emerged recently a sub-sector of the industry which is concerned only with the construction of intellectual property rights relating to IC designs. These firms design only logic functions without circuit layouts, and act in consultation with both small and large IC design firms in order to ensure patents are granted for the new chip protocol designs. The number of firms involved in this stage of the production process has grown enormously during the last two decades, with small design-oriented firms tending to be clustered in locations such as Silicon Valley. It is this part of the industry which has received so much academic attention. Yet, there are still many IC design activities which take place within vertically-integrated semiconductor producers both inside and outside of Silicon Valley.

The second stage of the process is the wafer process, the technology of which is determined by materials science. At this stage of the production process the circular

silicon wafers, produced by specialist chemicals firms, are subjected to lithography. This is a process whereby ultra-violet light is used to illuminate certain parts of the wafer, according to the mask design, in order to bring about chemical changes within certain parts of the wafer. The wafers are then etched and treated, thereby removing the parts of the wafer subjected to the lithography. After as many as fifteen stages of lithography and treating, the result is a three-dimensional silicon structure. This stage of the semiconductor production process can be compared to the plate-making and phototype process which takes place in the book printing industry.

The final stage of the wafer production process is that of the wafer assembly process. Here, the circular wafers which have been subjected to lithography and treating are extracted and dissected into many small square chips, each of which is then framed in plastic or ceramics for insulation and protection. This stage of the chip production process is the equivalent of the book binding process within the book publishing industry. The level of technology of the second and third stages of the wafer and assembly process is defined in terms of the minimum processing rule and the wafer size. The minimum processing rule is the definition of the level of miniaturization of the technology, and the wafer size is the size of the individual silicon wafers which can be produced and then dissected to produce chips. The smaller is the minimum processing rule and the greater is the wafer size, the more advanced is the technological generation. In terms of technology, the second and third stages of the semiconductor production process are just as important to the semiconductor industry as the first stage, and the product life-cycles are just as short. Different minimum processing rules and wafer sizes represent completely different generations of technology.

The majority of these second and third stage activities tend to be carried out by two groups of firms in more geographically dispersed locations outside of the US (Arita and McCann 2002a,b), and this may explain why these sectors have received relatively little academic interest. The first group of firms undertaking the wafer and assembly processes are the vertically-integrated semiconductor producers such as Intel and NEC, which undertake all of their own chip design and manufacturing activities. Firms such as NEC, Philips, Fujitsu and Motorola, which also manufacture finished goods, produce for internal demand as well as for other consumer firms, whereas firms such as Intel produce entirely for external customers. The common feature of the production of these firms is high volumes. The second group of firms undertaking the wafer and assembly processes are the specialist East Asian sub-contracting IC manufacturing firms. These are primarily Taiwanese, Japanese and Korean firms. They are comprised of a small number of specialist large firms, such as the Taiwan Semiconductor Manufacturing

Company, which have both the capacity to produce ICs in large numbers, and also the technology to allow both the high degree production specificity and flexibility required to manufacture custom-designed ICs.

Having discussed the nature of the semiconductor industry, in the next section we will look at the relationship between technological change and spatial industrial organization in the case of the semiconductor manufacturers who are located in the US and Europe. In particular we will focus on those firms which carry out the second and third-stage wafer process and assembly activities. The object of this exercise is to assess the extent to which orthodox product life-cycle approaches can broadly account for the technology-space relationship.

4.Data, Methodology and Results

The data we employ comes from the 2000 Nikkei compendium of the semiconductor industry, and provides individual plant and production line data for every semiconductor firm located within the US and Europe. The total number of such firms in the US is 37, and these firms account for 64 individual plants and 147 production lines. The total number of firms in Europe is 21, and these firms account for 40 individual plants and 79 production lines.

In terms of general establishment data, the Nikkei compendium provides us with the location details of each plant. For technology indices, the Nikkei compendium provides us with information on the minimum processing rule and the wafer size of the products produced at each location. In the case of the minimum processing rule, a smaller size represents a newer vintage of technology, whereas in the case of the wafer size, a larger size represents a newer technology. Nikkei also provide us with details of the wafer processing capacity, of the plant in terms of the total number of silicon wafers produced annually. As far as we are aware, such detailed semiconductor technology data has never before been employed statistically by applied economists.

With our technology, plant and spatial data we can now begin to investigate the relationship between geography and the implementation of technology within the wafer processing component of the semiconductor industry. Following an orthodox product-cycle argument we can hypothesize that different generations of semiconductor technologies will be spatially differentiated within the semiconductor industry. In particular, we would expect that the most recently developed products requiring the most advanced, miniaturized and newer production technologies will tend to be implemented at more central locations. In terms of technology indices, more advanced generations of technology are represented by smaller minimum processing rules and

larger wafer sizes. On the other hand, more mature vintages of product and process technologies would be expected to be implemented in more geographically peripheral locations exhibiting lower wage rates. The reason for this is that less advanced technology products will have become rather more standardized and easier to mass produce than more recent higher technology products. Moreover, increasing production quantities also imply the need for larger plants with larger land and labour requirements. This will provide an incentive for such plants to be located in lower wage and land price regions. Therefore, we ought to observe something of a positive correlation between increasingly mature vintages of a technology, the location of the product and process technology implementation, and the level of geographic peripherality of the establishment.

In order to test for an association between the level of geographical peripherality and the vintage of technology implemented, we employ a diagrammatic approach. Figure 2 describes the distribution of wafer production lines of semiconductor firms in the US and Figure 3 describes those in EU. First, we classified all the production lines into 5 classes according to the levels of technology, by combing the two production technology indices (the minimum processing rule and the wafer size) through the cluster-analysis methodology. Second, we also classified them into 9 classes according to the levels of production capacity of each line in terms of the total number of 200 mm silicon wafers equivalent produced monthly.

In the two diagrams, each circle represents each individual production line, with the information of the class of the production technology and that of the production capacity of each production line. The class of the production technology is described by the brightness of the black and white. Black color represents the more advanced level of technology and white represents the less advanced level. The latest level is exceptionally described by a star shape. The class of the production capacity is described by the size of each circle.

The results of the diagrams apparently demonstrates that we cannot find any support for the orthodox product-cycle argument. It is impossible to discover certain dominant “central places” for both of the diagrams. As for the US case, some places such as Silicon Valley, Oregon state , Texas state and New York state seem to be core places of the sub-regional clusters, since there are both concentrations of the production lines and also the lines of the latest technology are located. Nevertheless, in general, locations characteristics of the production lines are heterogeneous and any clear association cannot be observed between the level of geographical peripherality and the vintage of technology implemented. Therefore, it may be that the spatial patterns of technological

implementation within the semiconductor industry are determined primarily by factors not included in product-cycle type specification. These issues will be discussed in the next section.

5.Discussion

The alternative explanation for our lack of support for the product-cycle model within the semiconductor industry is that the wafer processing activities of the industry is comprised almost entirely of plants which are part of vertically-integrated hierarchical organizations, and the relationship between technology and geography in this industry depends on the spatial organization of these vertically-integrated firm hierarchies. These are points we will now consider.

Examples of the spatial organization of the 2 semiconductor firms, Intel and Royal Philips Semiconductor are shown in Figure 4 and 5. Our data for Intel here are based on 1994 observations (International Semiconductor Cooperation Center (INSEC), 1995). Intel is a firm based in Silicon Valley. As we see in Fig. 4, within the US, Intel exhibits a cluster of plants undertaking both R&D and wafer-processing activities in the area surrounding the location of the headquarters of the firm, and also in other US locations. Intel also has significant overseas R&D and wafer-processing investments. The spatial–organizational pattern of Intel is typical of the spatial investment patterns of US vertically integrated semiconductor producers (Arita and Fujita, 2001; Arita and McCann, 2002). Within the US, there are a large number of locations undertaking semiconductor production activities. Almost all of these activities are either in the R&D or wafer-processing activities, i.e., the first and second stages of the production process. These activities are often clustered together around the headquarters locations of the companies, but such clusters are not exclusively in these areas. Moreover, within the US, not all plants are located in spatial clusters, but are often individually sited in a range of locations. Whether or not a firm has an R&D facility in Silicon Valley depends largely on the founding location of the firm. In terms of overseas operations, significant proportions of the corporate R&D and wafer-processing activities, as well as all wafer assembly activities, take place outside of the US. The general pattern described in this example is broadly replicated in the cases of all the other major US vertically integrated semiconductor firms such as Motorola, Texas Instruments, National Semiconductor and Advanced Micro Devices (Arita and Fujita, 2001; Arita and McCann,2002). As for Royal Philips Semiconductors, it is one of the product divisions of Royal Philips Electronics based in Amsterdam, the Netherlands. Our data for this company is based on 2000 observations (Nikkei compendium 2000). Philips has its semiconductor process

technology research laboratory in Leuven, Belgium (not specified in Figure 5) and 7 major wafer-plants in Europe, 3 wafer plants in the US and 5 assembly plants in South-East Asia. The general pattern described in this example is broadly replicated in the cases of other major European vertically integrated semiconductor firms such as STMicroelectronics and Infineon Technologies AG.

The location behaviour of these firms is indicative of traditional multiplant location considerations in which activities are spatially differentiated across local labour markets according to the skill requirements of the various activities. Further evidence in support of these conclusions comes from the location behaviour of the overseas facilities of these firms. Such plants rarely have any R&D content, and are generally located in areas which already exhibit some specialization in the semiconductor industry. These considerations lend support to the argument that the location decisions regarding the placing of these facilities is based on orthodox multiplant–multinational lines, in which access to a suitable local labour force is a major consideration. For the vertically integrated semiconductor firms, their locational behaviours are therefore simply the result of orthodox multiplant locational considerations. Descriptions of this particular industry based on product-cycle model, thus, will be very misleading.

6.Conclusion

This paper has discussed the various sub-sectors of the semiconductor industry, and applied a simple product-cycle model to the case of the wafer-processing part of the industry based within Japan. The data we employ is some of the most detailed and disaggregated technological data available for such an industry. The models presented here find little or no association between the implementation of technological innovations and the location of the activity. There is some evidence for industrial clustering between local establishments, but this takes place within a tight organizational logic designed specifically to rule out information externalities (Arita and McCann 2002a,b). The only evidence we do find is that the larger capacity facilities will tend to be in the more geographically peripheral, lower wage and land-price regions, an observation consistent with orthodox location theory considerations. The explanation we offer for these observations is that the spatial patterns of production in the semiconductor industry, are dominated by issues of decision-making and control within vertically-integrated hierarchical organizations. The arguments presented here suggest that the location behaviour of these vertically-integrated parts of the global semiconductor industry are governed primarily by traditional multiplant and multinational location considerations, in which different activities or groups of activities

are located in different regions for different reasons, subject to the organizational arrangements of the firm. Observations contrasting the behaviour of Silicon Valley and other parts of the semiconductor industry (Saxenian 1994) are of very limited analytical use for more general industry-organization discussions.

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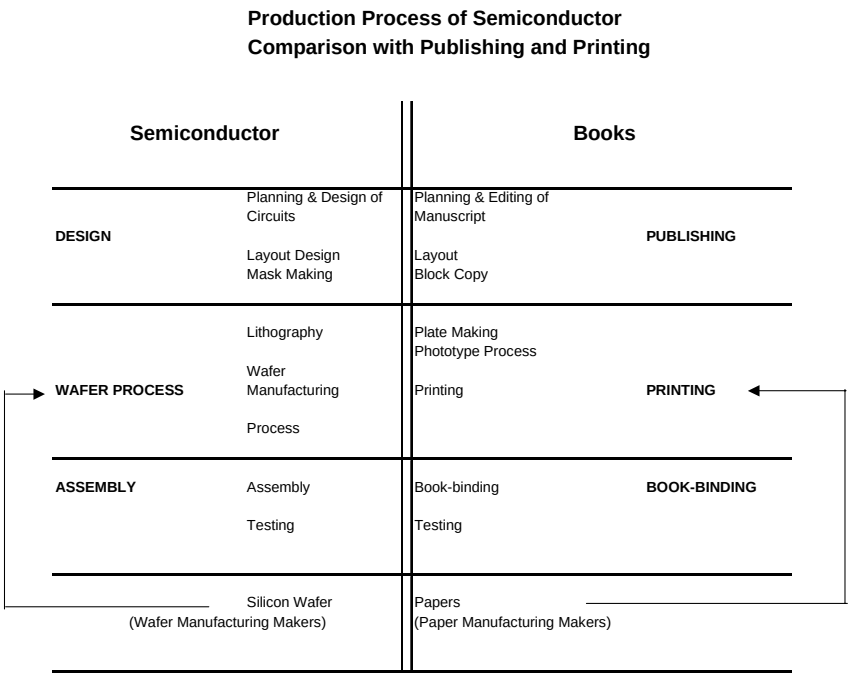

Figure 1. Production Process of semiconductor: comparison with book publishing and printing

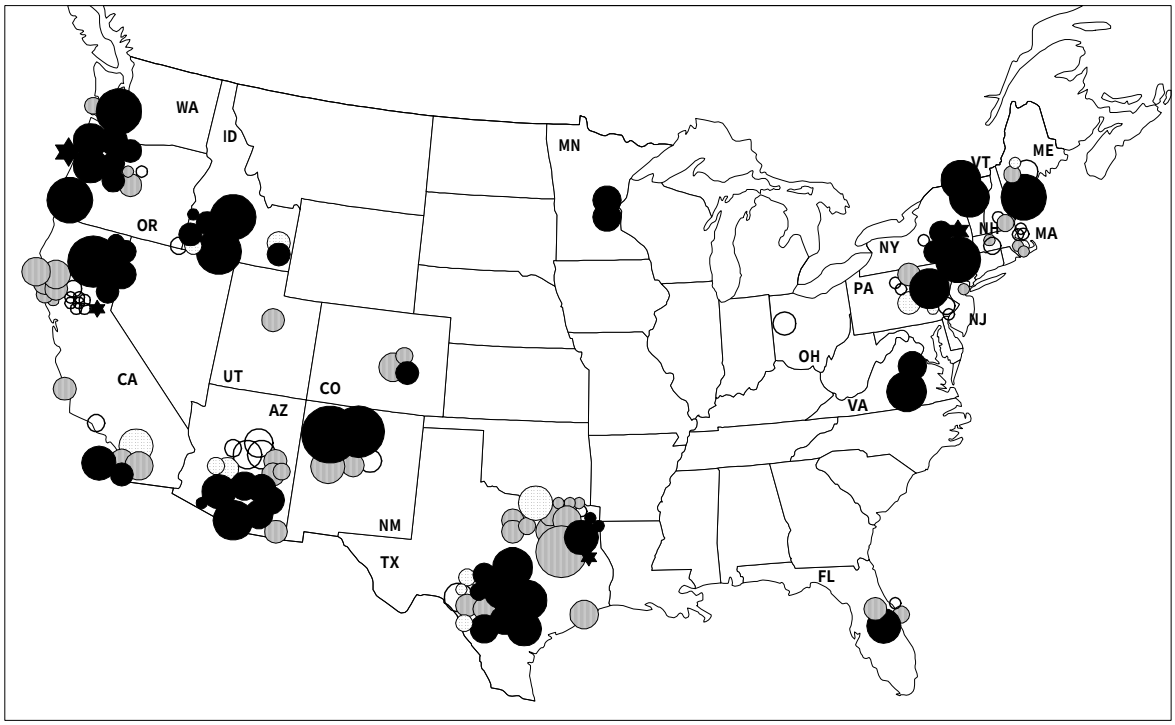

Fig. Distribution of Wafer Production Lines of semiconductor firms in USA

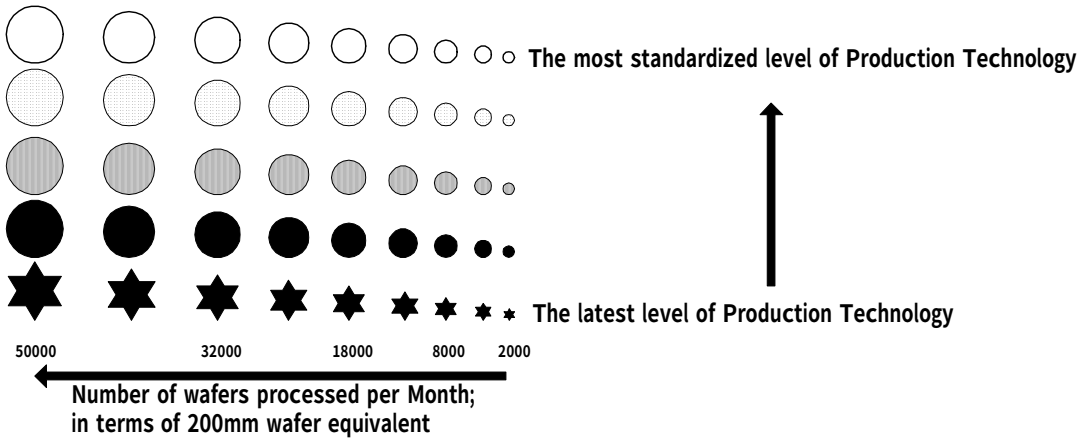

Figure 2. Distribution of wafer production lines of semiconductor firms in the US

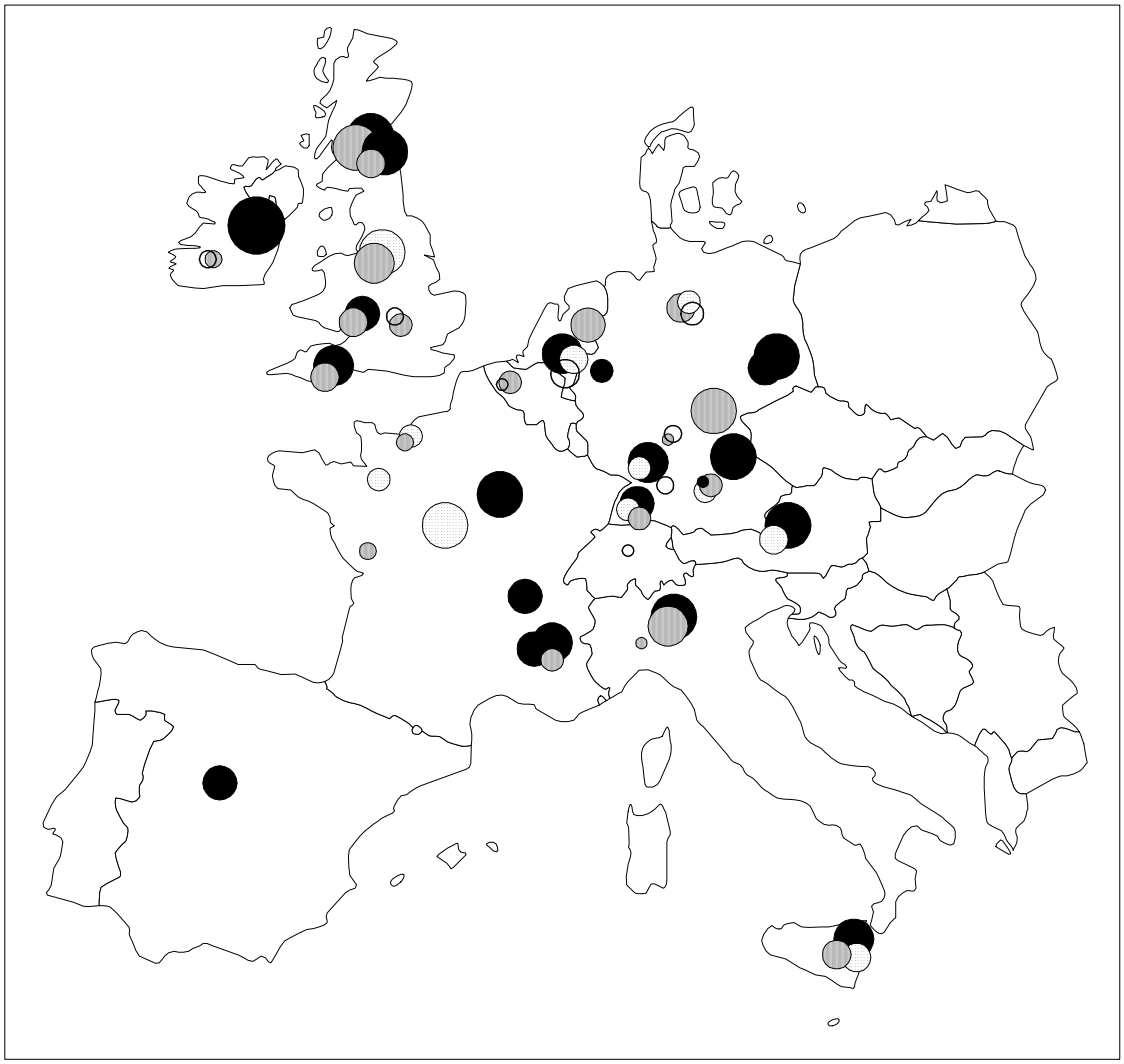

Fig. Distribution of Wafer Production Lines of semiconductor firms in EU

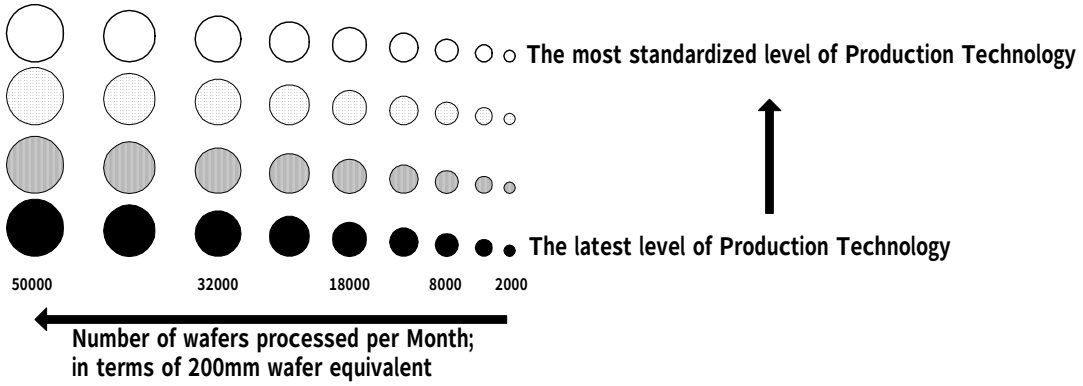

Figure 3. Distribution of wafer production lines of semiconductor firms in Europe

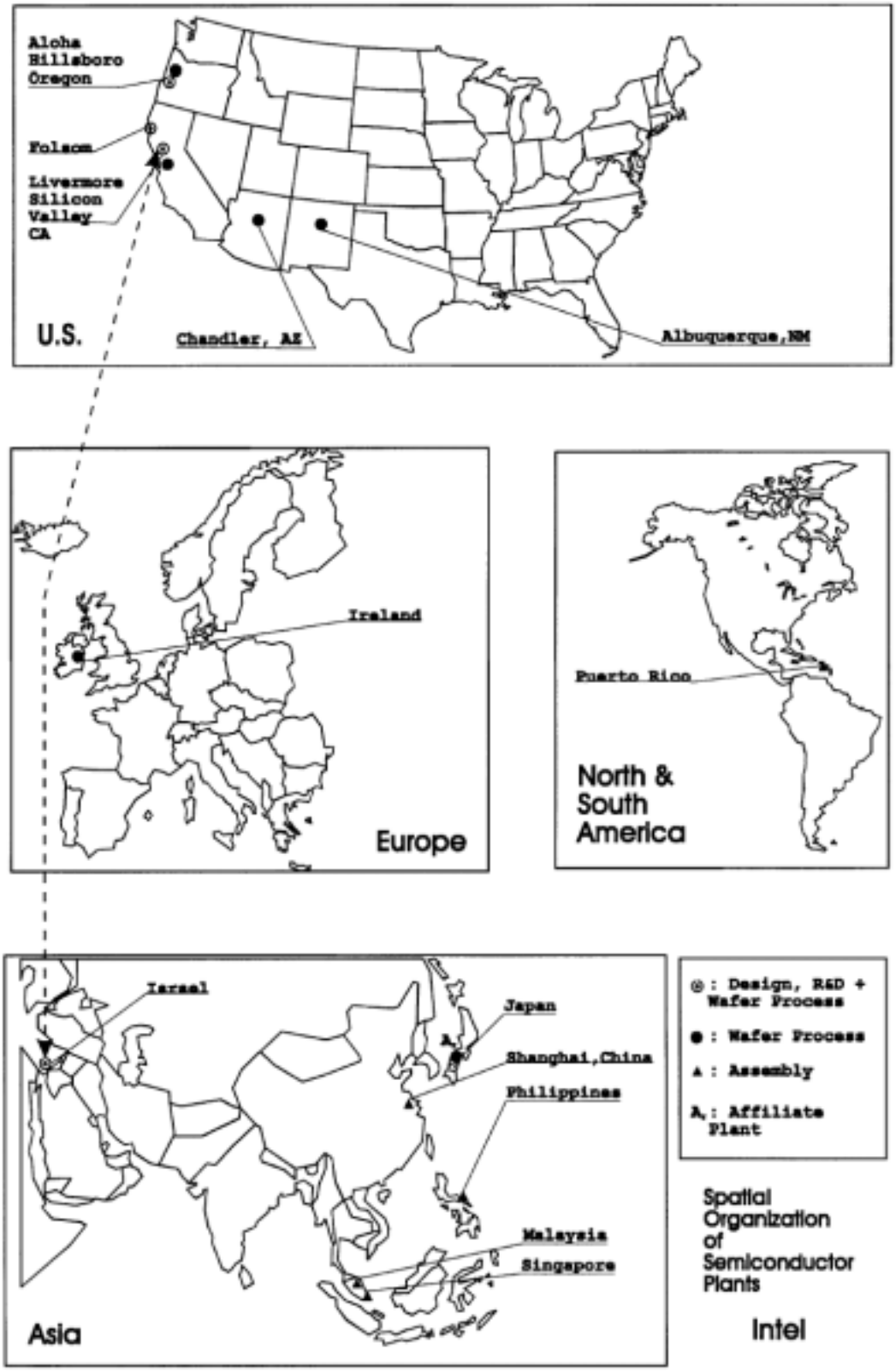

Figure 4: The Spatial Organization of semiconductor plants at Intel(1994)

Figure 5: The Spatial Organization of semiconductor plants at Royal Philips (2000)